

ABSTRACT OF THE DISCLOSURE

A memory cell with reduced short channel effects is described. A trench region is formed in a semiconductor substrate. A source region and a drain region are formed on opposing sides of the trench region, wherein a bottom of the source region and a bottom of the drain region are above a floor of the trench region. A gate dielectric layer is formed in the trench region of the semiconductor substrate between the source region and the drain region. A recessed channel region is formed below the trench region, the source region and the drain region. A control gate is formed on the semiconductor substrate above the recessed channel region, wherein the control gate is separated from the recessed channel region by the gate dielectric layer.

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